AN ADVANCED HYBRID ASSEMBLY TECHNIQUE FOR 40GBIT/S-MODULES INCLUDING SURFACE AND FEED-THROUGH CAPACITORS

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ABSTRACT

Experimental 40Gbit/s ETDM transmitter and receiver modules for optical fiber link applications were developed. To obtain the essential extreme broad bandwidth the GaAs-chips are connected by self-supporting leads to ceramic thinfilm circuits which shows nearly reflection- and discontinuity-free connections up to millimeter-wave frequencies. In addition the use of hybrid integrated surface and coaxial feed-through capacitors results in low impedances and ultra broadband bypasses.

INTRODUCTION

The higher bit rates are needed for modern telecommunication use the more difficult become assembly and interconnecting techniques. In contrast to small- and medium-band microwave and millimeterwave applications most of the digital signal processings have to be performed in the basic band and therefore need low cut-off frequencies down to DC. Problems like frequency dispersion of micro striplines, frequency dependence of parasitic impedances, and transforming characteristics of any finit length of layer must be solved.

A good and meanwhile proved and reliable tool for multi-gigabit rates and millimeterwave interconnecting and assembly is the chip-in-board mounting of semiconductor circuits and components into ceramic substrates in combination with hybrid integrated techniques and the "Reverse Beam-Lead"-interconnecting method. High-speed modules for optical fiber transmission systems working at 40GHz demonstrate the advantages of this technology.

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40 GBIT/S-MODULES

Both, a 40Gbit/s 2:1-multiplexer and a 40Gbit/s 1:4-demultiplexer were built up and tested. The GaAs-chips were developed by Fraunhofer Institut, Freiburg/Germany, and use a 0.2µm source coupled FET logic. As an example Fig. 1 shows the block diagram of the 1:4-demultiplexer, which is inserted in a hybrid thinfilm circuit (Fig. 2a). Since all broadband inputs and outputs are of differential type, coupled microstrip lines can be used to reduce the required space for 50Ω microstrip lines around the chip, see details in Fig. 2a.

CAPACITORS

Bypassing of power supply connections is done by hybrid integrated surface capacitors and by coaxial feed-through capacitors which could be integrated into the via holes. In Fig. 2b these capacitors are arranged inside the drillings of the blue (power supply layers) metallisation layers. Additional surface capacitors are not shown in the figure, they overlay red (ground layers) and blue layers.

The high frequency characteristics of the coaxial capacitors were measured with the aid of an S-parameter equipment (HP 8510/8517). They were placed in the middle of an 1 inch long 50Ω microstrip line (Fig 3b). The calculated equivalent circuit can be described roughly by the series connection of C = 2.3pF, R = 0.1Ω

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and L = 7pH. Because the inductance is given by length and diameter of the drilling the resonance frequency must be influenced by the value of the capacitance, what can be done rather easily by varying the thicknes of the dielectric material. In Fig 3a the measured characteristic of a real coaxial capacitor (blue line) is compared with the characteristic of the equivalent circuit (red line) and an ideal capacitor of 2.3pF (green line). The resonance near the bit repetition rate gives an additional and wanted effect for the shunting quality of this component.

ASSEMBLY

The described 40Gbit/s modules are produced by means of usual thin film photolithographic technology on polished Al_2O_3-ceramics. The thickness of substrate is 254µm. To manufacture the required MIC the semi-additive technology is used:

1. Basic metallizations (Cr/Au) are manufactured by sputtering.
2. The final tracks (Au) are generated by additive galvanic plating. For this purpose a conventional cyanide gold electrolyte is used.
3. Removal of remaining Au/Cr layer by a corrosive.

To realize the "Reverse Beam-Lead" CIB chip embedding and interconnection technique the used chip-sized substrate openings are cut out by a laser at first. It is advantageous to use an excimer laser for it. The cut-outs are following filled with a suitable material. Indium proved to be capable for this purpose. Then the microstrip line structure containing leads for chip interconnecting is produced by additive galvanic plating. After removal of the filling material a microstrip line device with chip interconnection leads is obtained. The dice can be inserted by face-down mounting with a flip-chip bonder [3], [4].

To manufacture the described integrated capacitor devices also the thin film technology is used. After producing of the basic electrode by photolithographic structuring/additive galvanic plating (Cr/Au//Au) the dielectric layer is realized. For this purpose a photosensible polyimid is used as dielectric applied by spin coating (for planar capacitor) or suck applying (for the feed-through capacitor). The dielectric constant is about $\varepsilon_r = 3.3$. As next step the top electrodes are produced. For it the semi-additive technology is used, too (Cr/Au//Au). After forming the top electrodes the hybrid circuit is complete. In figure 4a and figure 4b the constructon of a planar capacitor is shown. Onto basic electrodes as part of the microstrip line the dielectric is generated. Over it the top electrodes are formed. Figure 5a and figure 5b show a feed-through capacitor. In this case the capacitor is assembled inside of a through hole. The basic construction is identical with a planar capacitor. In order to achieve a capacitance of such blocking capacitor of C = 2..3pF it is necessary to apply a thin very even polyimid film. The thickness has to be about 3..5µm. The leads for interconnecting of chips are extensions of the top electrodes, too. Figure 6 shows a detail of the 40Gbit/s multiplexer module manufactured by means of "Reverse Beam-Lead" technology.

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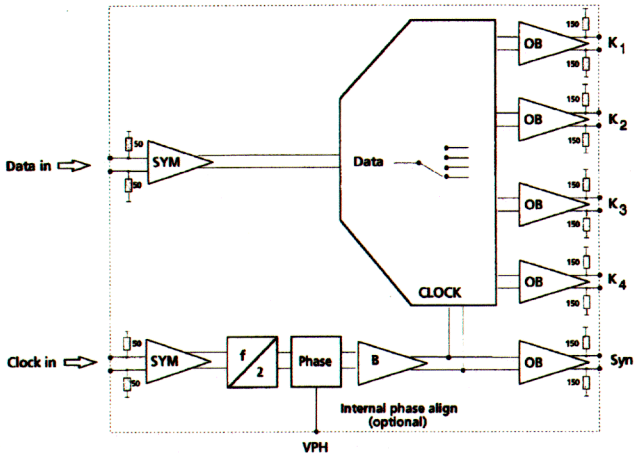

Fig1
Block diagram of the GaAs 1:4-demultiplexer for the 40 Gbit/s input data. Clock frequency is 20 Ghz. By means of Vph clock phase can be changed. The chip has overall dimensions of 1.5 by 2.0 mm^2 and consists of 470 active components.

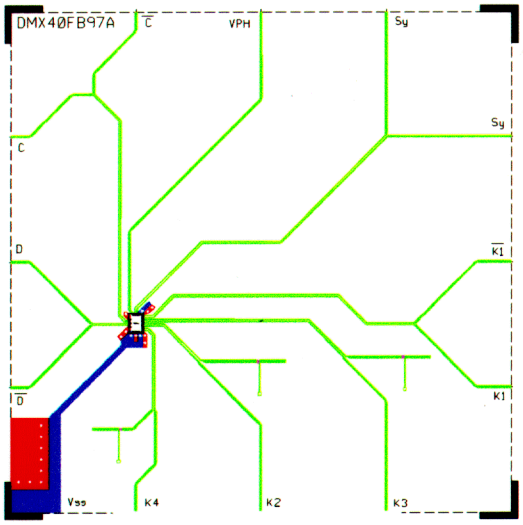

Fig2a
Layout of the 40 Gbit/s 1:4-demultiplexer module. The size of the hybrid integrated thinfilm circuit is 2 "by 2".

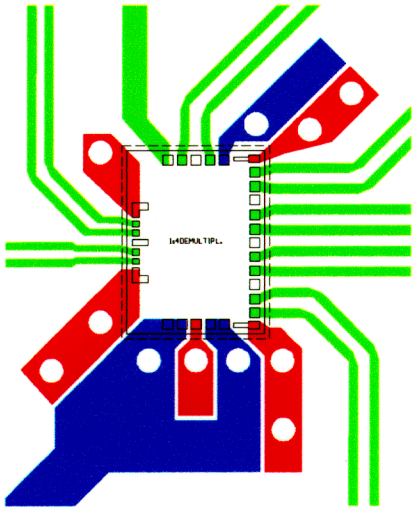

Fig2b
Detail of the hybrid circuit; the chip connections are "reverse beam-leads", the drillings in the blue areas contain coaxial bypass capacitors.

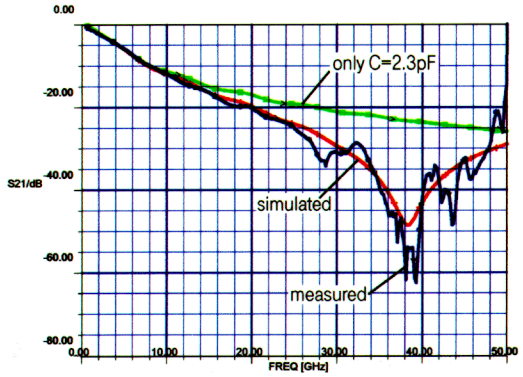

Fig3a
High frequency characteristics of a coaxial bypass capacitor (S_{21} parameters). The resonance frequency is about 40 Ghz.

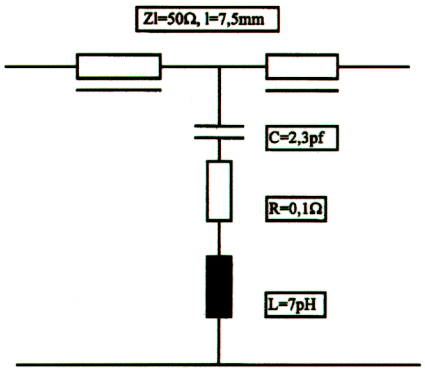

Fig3b
Equivalent circuit of the coaxial capacitor (microstrip lines are for measuring purpose)

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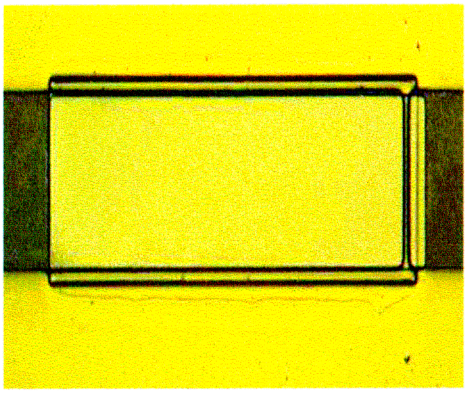

Fig.4a: Microstrip line with planar capacitor (dielectric: polyimid [5µm], width: 254µm).

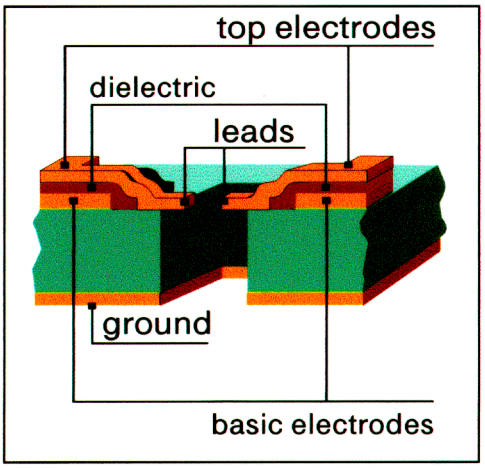

Fig.4b: Manufactured CIB strip-line device containing planar capacitors.

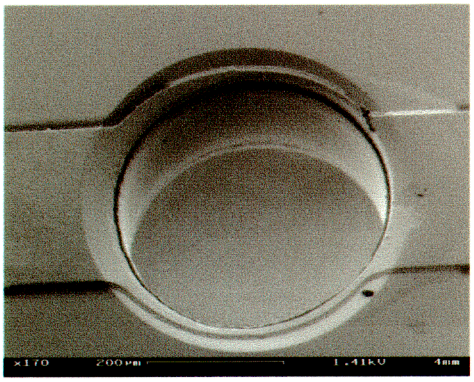

Fig.5a: Microstrip line with feed-through capacitor (dielectric: polyimid [3µm], diameter: 300µm).

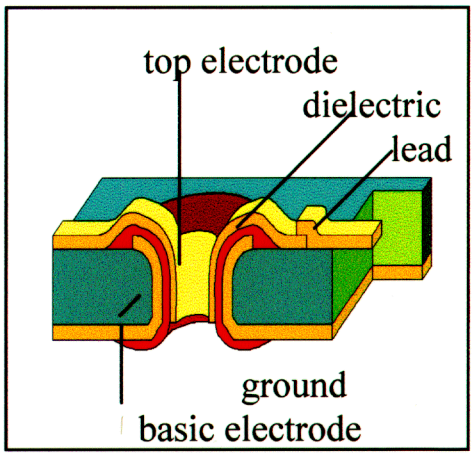

Fig.5b: Manufactured CIB strip-line device containing a feed-through capacitor.

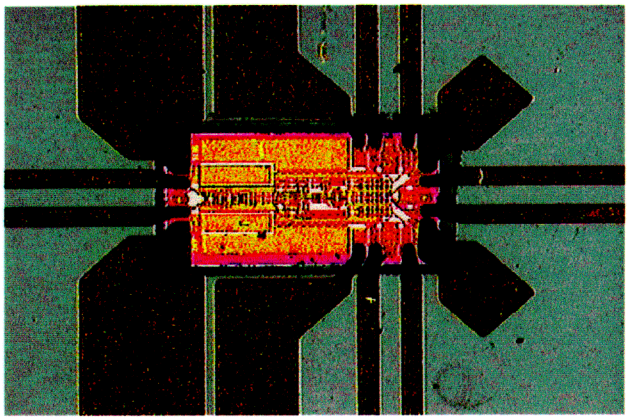

Fig. 6: Detail of the 40Gbit/s GaAs-Multi-plexer-Module. 40Gbit/s coupled output-lines go to the left, 20 GHz coupled clock-lines to the right.